

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application

- 1 1. (Original) A non-volatile semiconductor memory
- 2 allowing information to be electrically written thereto and
- 3 information stored therein to be electrically erased,
- 4 comprising: a memory array including a plurality of non-
- 5 volatile memory cells each used for storing information as
- 6 a threshold voltage thereof, said non-volatile
- 7 semiconductor memory allowing information to be written in
- 8 predetermined units and stored information to be erased in
- 9 said units,
- 10 wherein, in the event of a power-supply cutoff in the
- 11 course of a write or erase operation carried out on any
- 12 specific one of said non-volatile memory cells, said write
- 13 or erase operation currently being executed is discontinued
- 14 and a write-back operation is carried out on said specific
- 15 non-volatile memory cell to change said threshold voltage
- 16 of said specific non-volatile memory cell in a direction to
- 17 raise said threshold voltage.

1 2. (Original) A non-volatile semiconductor memory
2 according to claim 1, including an external terminal for
3 receiving a predetermined control signal,
4 wherein, in accordance with a change in said control
5 signal inputted to said external terminal, an occurrence of
6 a power-supply cutoff is detected, and a write-back
7 operation is carried out.

1 3. (Original) A non-volatile semiconductor memory
2 according to claim 2,
3 wherein said memory cells are each a memory cell with
4 said threshold voltage thereof increased to a high level by
5 a write operation and decreased by an erase operation, and
6 wherein in the event of a power-supply cutoff in the
7 course of a write or erase operation carried out on any
8 specific one of said non-volatile memory cells, said
9 threshold voltage of said specific non-volatile memory cell
10 is examined to determine whether or not said threshold
11 voltage has decreased to a predetermined level or a level
12 even lower than said predetermined level and, if said
13 threshold voltage has decreased to said predetermined level
14 or a level even lower than said predetermined level, a bias

15 voltage is applied in a direction to raise said threshold
16 voltage of said specific non-volatile memory cell.

1 4. (Original) A non-volatile semiconductor memory
2 according to claim 3, wherein, in an operation to update
3 information stored in any selected one of said non-volatile
4 memory cells, said threshold voltage of said selected non-
5 volatile memory cell is once changed to a low level before
6 being restored back to a high level.

1 5. (Original) A non-volatile semiconductor memory
2 according to claim 4, wherein said memory array is a memory
3 array having a plurality of memory columns each including a
4 plurality of said memory cells connected in parallel.

1 6. (Original) A non-volatile semiconductor memory
2 according to claim 5, further including a flag comprised of
3 a non-volatile memory cell for storing an occurrence of a
4 power-supply cutoff in the course of a write or erase
5 operation.

1 7. (Original) A non-volatile semiconductor memory
2 according to claim 6, wherein said flag is provided for
3 each write-operation unit.

1 8. (Original) A non-volatile semiconductor memory
2 according to claim 6,
3 wherein address decode is configured to be
4 hierarchically carried out,
5 wherein there is provided a first flag group comprised
6 of flags respectively corresponding to a plurality of first
7 memory-cell groups selected by decode of a high-order
8 address, and a second flag group comprised of flags
9 respectively corresponding to a plurality of second memory-
10 cell groups common in low-order address in said first
11 memory-cell group, and
12 wherein when a power-supply cutoff occurs in the
13 course of write or erase operation with respect to the
14 corresponding first and second memory-cell groups is
15 performed, said first flag group and said second flag group
16 are made to be a set state.

1 9. (Original) A non-volatile semiconductor memory
2 according to claim 5, further including a non-volatile

3 memory circuit for storing an address indicating a memory
4 cell serving as a target of a write or erase operation in
5 the event of a power-supply cutoff in the course of said
6 write or erase operation.

1 10. (Original) A non-volatile semiconductor memory
2 according to claim 9, further including a flag, which is
3 used for indicating that an operation mode is a write
4 operation mode or an erase operation mode if a power-supply
5 cutoff occurs while an operation is being carried out in
6 said write operation mode or said erase operation mode
7 respectively.

1 11. (Original) A non-volatile semiconductor memory
2 according to claim 9, wherein, at power supply starting, an
3 address stored in said non-volatile memory circuit is read
4 to a predetermined register.

1 12. (Original) A non-volatile semiconductor memory
2 according to claim 11, wherein, in accordance with a
3 predetermined command code or predetermined control signal
4 received from an external source, the address stored in
5 said register is outputted to outside.

1 13. (Original) A non-volatile semiconductor memory
2 allowing information to be electrically written thereto and
3 information stored therein to be electrically erased,
4 comprising: a memory array including a plurality of non-
5 volatile memory cells each used for storing information as
6 a threshold voltage thereof; and an internal power-supply
7 circuit for generating an internal power-supply voltage
8 required for internal operations on the basis of an
9 external power-supply voltage received from an external
10 source, said non-volatile semiconductor memory allowing
11 information to be written in predetermined units and stored
12 information to be erased in said units,
13 wherein said internal power-supply circuit is
14 implemented into a configuration for generating said
15 internal power-supply voltage varying in accordance with
16 the level of said external power-supply voltage and, in the
17 event of a power-supply cutoff in the course of a write or
18 erase operation carried out on any specific one of said
19 non-volatile memory cells, said write or erase operation
20 currently being executed is discontinued and a write-back
21 operation is carried out on said specific non-volatile
22 memory cell to change said threshold voltage of said

23 specific non-volatile memory cell in a direction to raise
24 said threshold voltage.

1 14. (Original) A non-volatile semiconductor memory
2 according to claim 13, wherein said internal power-supply
3 circuit has a charge-pump circuit capable of changing the
4 number of charge-pump stages, and said charge-pump circuit
5 is implemented into a configuration allowing a voltage-
6 raising capacitor at a voltage-raising stage not
7 contributing to a voltage-raising operation to serve as a
8 smoothing capacitor for a small number of said charge-pump
9 stages.

1 15. (Original) A non-volatile semiconductor memory
2 according to claim 14, further including a power-supply
3 voltage detection circuit for detecting a level of a power-
4 supply voltage received from an external source,
5 wherein said charge-pump circuit changes the number of
6 said charge-pump stages in accordance with said level
7 detected by said power-supply voltage detection circuit.

Claims 16-20 (Cancelled)